ABSTRACT

An apparatus and method of testing an integrated circuit by downloading a sequence of randomly weighted bits into a scan chain in which each bit has a distinctly determined weight generated in real-time by a weight generator. The weight generator has a switch controlled by a stored bit particular for each bit of the randomly weighted bits that determines the weight of the bit. The control signal is stored in a memory that is downloaded into the switch in synchronization with the generation of the bit. Preferably, the memory is on-die, and furthermore is a part of the integrated circuit.